ABSTRACT

A method and apparatus are disclosed for dynamically reducing clock skew among various nodes on an integrated circuit. The disclosed clock skew reduction technique dynamically estimates the clock delay to each node and inserts a corresponding delay for each node such that the clock signals arriving at each node are all in phase with a global clock (or 180° out of phase). Delays attributable to both the wire RC delays and the clock buffer delays are addressed. A feedback path for the clock signal associated with each node allows the round trip travel time of the clock signal to be estimated. When the length of the feedback path matches the length of the primary clock path, the clock skew present at the corresponding node can be estimated as fifty percent (50%) of the round trip delay time. Dynamic adjustments to the delay control circuit are permitted as operating conditions shift. Clock signals arriving at individual nodes on the integrated circuit remain in phase with the global PLL clock (PCK), regardless of variations in the operating voltage or temperature (or both).